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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,331	10/20/2003	Kiyoshi Takeuchi	IKM-01402	2732

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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,331	TAKEUCHI, KIYOSHI	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/516,073.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated October 20, 2003 in which claims 1-11 were cancelled has been entered of record.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/516,073, filed on March 1, 2000.

Claim Objections

3. Claim 12 is objected to because of the following informalities: on line 8, replace "cannel" with --channel--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12-17, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,184,083 to Tsunashima et al. Tsunashima teaches in figures 5A-D, 7A-D and 8A-D, a method of making a complementary integrated circuit comprising:

preparing a semiconductor substrate 101;

forming a region for forming an n-channel element and a region for forming a p-channel element on the substrate via an element isolation region 105 (see fig. 5A which shows on the right side of the figure the substrate 101 comprising two broad pillars, wherein the left-most pillar is a region where a p-channel device region is formed and the right-most pillar is a region in which an n-channel device is formed);

forming a dummy gate electrode 103 in each of the n- and p-channel regions (fig. 7A);

forming n-type diffusion regions 101b and p-type diffusion regions 101a in the n-channel and p-channel regions respectively;

forming an insulating film 107 over the entire surface of the substrate;

removing the dummy gate in the region for forming the p-channel element to create a first trench and filling the first trench with a gate electrode material (figs. 7B and 7C); and

removing the dummy gate in the region for forming the n-channel element to create a second trench and filling the second trench with a gate electrode material (figs. 8A and 8B).

Regarding claim 13, Tsunashima teaches that the source and drain regions are ion implanted using the dummy gate 103 as a mask (col. 9, lines 59-64) and it is considered inherent that when one region is being ion implanted to form its source/drain structures, the other region is covered with a resist film for if not, the implantation would be formed in both regions resulting in charge neutral source/drains. Regarding claim 14, Tsunashima teaches that insulating film 107 is formed on the entire surface of the structure and is removed to expose the upper surfaces of the dummy gates (paragraph bridging cols. 9-10). Regarding claim 15, Tsunashima teaches that after the dummy gates are removed from the first and second trenches, a gate insulating film 108 and 111 is formed in the trench such that the gate electrode material 109 and 112 is formed

on the gate insulating film (see figs. 7C and 8B). Regarding claim 16, Tsunashima teaches that the formation of the first and second gates is achieved by forming films 109 and 112 on the whole surface of the substrate and then polishing them (see figs. 7D and 8C, col. 10, lines 21-33, col. 11, lines 20-26). Regarding claims 17, 19 and 20, Tsunashima teaches that the gate electrodes are formed by a lower portion (e.g. 109 which is a p+ polysilicon and 112 which is an n+ polysilicon) having a specific work function and an upper portion 110 which is tungsten and has a low electrical resistivity.

5. Claims 21, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,489,191 to Shao et al. Shao teaches in figures 1-4 a method of manufacturing a complementary integrated circuit, comprising:

preparing a substrate 11;

forming a region for forming an n-channel element (p-well) and a region for forming a p-channel element (n-well) on the substrate via an element isolation region 12;

forming an insulating layer 30 over the entire surface of the substrate (fig. 1A);

selectively removing the insulating film to form first and second trenches 35 in the n-channel and p-channel element regions respectively and filling the trenches with gate electrode material 40and 50;

removing the insulating film (fig. 4); and

forming n-type and p-type diffusion regions in the n-channel and p-channel regions respectively (fig. 4, col. 5, lines 16-40).

Regarding claim 23, Shao teaches that the gates are made by forming a film made of the gate electrode material over the whole surface of the substate and polishing the film so to expose the upper surfaces of the gates (fig. 3, paragraph bridging cols. 4-5). Regarding claim 24, Shao teaches that the gate electrode material may be chosen from doped polysilicon, tungsten or polysilicon with overlying silicide any of which have work functions "close" to that of either n- or p-doped poly.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 18 and 25 are respectively rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunashima and Shao in view of 6,130,123 to Liang et al. Tsunashima and Shao taught the methods of claims 12 and 21 respectively but did not expressly teach the claimed composition of the first and second gate electrodes. Liang teaches that the first and second gate electrodes of a CMOS device may be formed of zirconium and nickel respectively.

Tsunashima or Shao and Liang are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Tsunashima or Shao using the materials taught by Liang. The motivation for doing so is that by choosing the appropriate gate material, lower threshold voltages may be achieved (col. 1, lines 54-57). Therefore, it would have been obvious to combine Tsunashima and Liang or Shao and Liang to obtain the invention of claims 18 and 25.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shao in view of 6,291,282 to Wilk et al. Shao taught the method of claim 21 but did not expressly teach that the gate insulating film was formed in the trench after the trench was formed. Wilk teaches in figure 3d a method wherein a trench is formed and a gate insulator 324 is formed after the trench is formed such that the gate material 326 is formed on the gate insulator.

Shao and Wilk are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the gate insulator forming method of Wilk in the process of Shao. The motivation for doing so, as is taught by Wilk, is that if the gate insulator is not comprised of the desired material, it may be removed and replaced with a chosen material (col. 5, lines 8-10). Therefore, it would have been obvious to combine Shao and Wilk to obtain the invention of claim 22.

8. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shao in view of Tsunashima. Shao taught the method of claim 21 but did not expressly teach the claimed gate materials. Tsunashima teaches that the gate electrodes of the NMOS and PMOS transistors may comprise a lower section of n-type 112 or p-type 109 doped polysilicon and an upper section of a low resistivity material 110.

Shao and Tsunashima are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to practice the process of Shao using the materials taught by Tsunashima. The motivation for doing so, as is taught by Tsunashima, is that such materials allow a gate formed having a damascene structure such that plasma damage is minimized and no heat treatment is necessary. Therefore, it

would have been obvious to combine Shao and Tsunashima to obtain the inventions of claims 26 and 27.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional art teaches methods of forming CMOS devices using dummy gates and trenches formed in insulating layers without dummy gates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER